

FIG. 1B

V[1:0] (OUTPUT STATE)	A	B	Y
LL (Hi-Z)	don't care	don't care	X
LH (1.2V)	L	L	H
HL (1.5V)	L	H	H
HL (1.5V)	H	L	H
HH (1.8V)	H	H	L

FIG. 1C

TRANSITION OF INPUT SIGNALS		DELAY VALUE FOR EACH STATE OF V[1:0] (ns)		
V[1:0]	(A, B)	LH (1.2V)	HL (1.5V)	HH (1.8V)
≠LL	LH→HH	A1h(V1h)	A1h(Vh1)	A1h(Vhh)
	HH→LH	Ah1(V1h)	Ah1(Vh1)	Ah1(Vhh)
	HL→HH	B1h(V1h)	B1h(Vh1)	B1h(Vhh)
	HH→HL	Bh1(V1h)	Bh1(Vh1)	Bh1(Vhh)
LL→≠LL	XX	Vst(V1h)	Vst(Vh1)	Vst(Vhh)
≠LL→LL	XX	Voff(V1h)	Voff(Vh1)	Voff(Vhh)

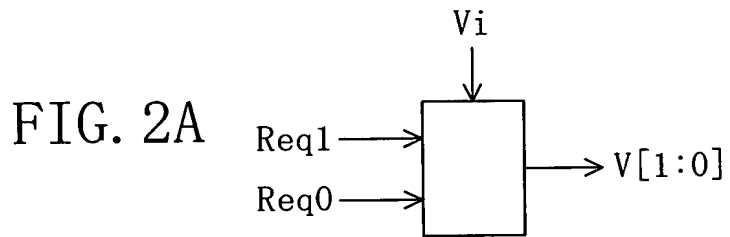


FIG. 2B

Vi (INPUT STATE)	Req1	Req0	V[1:0] (OUTPUT STATE)
L (Hi-Z)	don't care	don't care	LL (Hi-Z)
H (3V)	L	L	LL (Hi-Z)
	L	H	LH (1.2V)
	H	L	HL (1.5V)
	H	H	HH (1.8V)

FIG. 2C

TRANSITION OF INPUT SIGNAL		DELAY VALUE (ns)
Vi	(Req1, Req0)	
H	LL→LH LL→HL LL→HH	Vst
	LH→LL HL→LL HH→LL	Voff
	OTHER THAN THE ABOVE	Vtr
L→H	≠LL	Vist
H→L		Vioff

FIG. 3

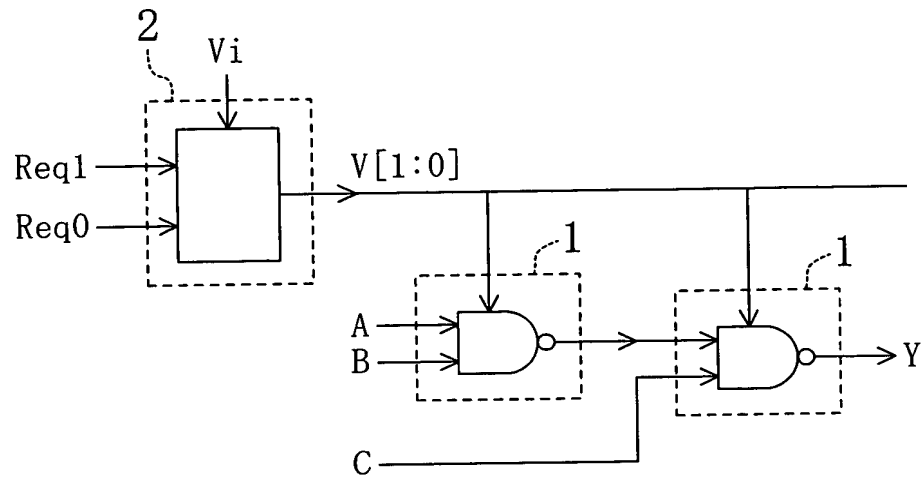


FIG. 4A

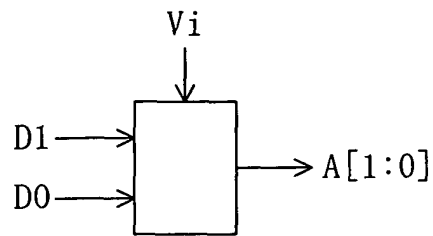


FIG. 4B

Vi (INPUT STATE)	D1	D0	A[1:0] (OUTPUT STATE)
L (Hi-Z)	don't care	don't care	X (Hi-Z)
H (3V)	L	L	LL (0.5V)
	L	H	LH (1V)
	H	L	HL (1.5V)
	H	H	HH (2V)

FIG. 4C

TRANSITION OF INPUT SIGNAL		DELAY VALUE (ns)
Vi	(D1, D0)	
H	ANY CHANGE OF STATE	Atr
L→H	ANY STATE	Ast
H→L	ANY STATE	Aoff

FIG. 5A

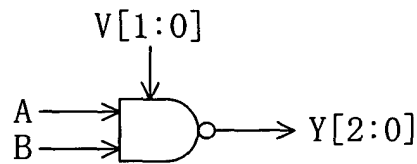


FIG. 5B

V[1:0] (OUTPUT STATE)	A	B	Y[2:0]
LL (Hi-Z)	don't care	don't care	XXX
LH (1.2V)	L	L	LHH
	L	H	LHH
	H	L	LHH
	H	H	LHL
HL (1.5V)	L	L	HLH
	L	H	HLH
	H	L	HLH
	H	H	HLL
HH (1.8V)	L	L	HHH
	L	H	HHH
	H	L	HHH
	H	H	HHL

FIG. 6A

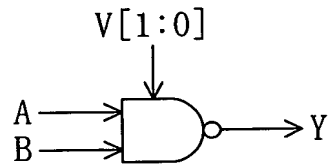


FIG. 6B

V[1:0] (OUTPUT STATE)	A	B	Y
LL (Hi-Z)	don't care	don't care	X
LH (1.2V)	L	L	H
HL (1.5V)	L	H	H
HL (1.5V)	H	L	H
HH (1.8V)	H	H	L

FIG. 6C

TRANSITION OF INPUT SIGNAL		DELAY VALUE FOR EACH STATE OF V[1:0] (ns)		
V[1:0]	(A, B)	LH (1.2V)	HL (1.5V)	HH (1.8V)
≠ LL	LH → HH	A1h(V1h)	A1h(Vh1)	A1h(Vhh)
	HH → LH	Ah1(V1h)	Ah1(Vh1)	Ah1(Vhh)
	HL → HH	B1h(V1h)	B1h(Vh1)	B1h(Vhh)
	HH → HL	Bh1(V1h)	Bh1(Vh1)	Bh1(Vhh)
LL → ≠ LL	XX	Vst(V1h)	Vst(Vh1)	Vst(Vhh)
≠ LL → LL	XX	Voff(V1h)	Voff(Vh1)	Voff(Vhh)

FIG. 6D WITHSTAND VOLTAGE: 1.7V

FIG. 7A
PRIOR ART

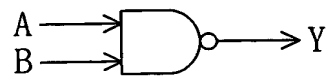


FIG. 7B
PRIOR ART

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

FIG. 7C
PRIOR ART

A→Y	DELAY VALUE AYns
B→Y	DELAY VALUE BYns

FIG. 8A

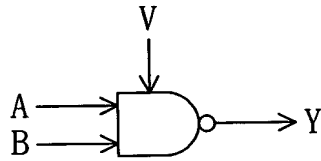


FIG. 8B

V	A	B	Y
L	don't care	don't care	X
H	L	L	H
	L	H	H
	H	L	H
	H	H	L

FIG. 8C

A→Y	DELAY VALUE AYns
B→Y	DELAY VALUE BYns
V→Y	DELAY VALUE VYns